Notice of Allowability	Application No.	Applicant(s)	
	10/801,072	KUCHEROV ET AL.	
	Examiner	Art Unit	
	Alan Diamond	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed February 13, 2006*.

2. ☒ The allowed claim(s) is/are *2-8 and 12-37*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *04242006* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Carl Reed on April 21 and 24, 2006.

In The Specification

In page 1, at the third line of paragraph 0001, after "November 27, 2002," please insert --now U.S. Patent 6,906,449,--.

In The Claims

1. (Cancelled)

2. (Previously Presented) The solid state energy converter of claim 17, further comprising a collector region in thermal communication with a cold heat exchange surface, the collector region being in electrical and thermal communication with the gap region.

3. (Previously Presented) The solid state energy converter of claim 2, wherein the gap region is adjacent to the collector region.

4. (Original) The solid state energy converter of claim 2, further comprising a first ohmic contact in electrical communication with the emitter region.

5. (Original) The solid state energy converter of claim 4, further comprising a second ohmic contact in electrical communication with the collector region.

6. (Original) The solid state energy converter of claim 5, wherein the first and second ohmic contacts close an electrical circuit through an external load for heat to electricity conversion.

7. (Original) The solid state energy converter of claim 5, wherein the first and second ohmic contacts close an electrical circuit through an external power source for electricity to refrigeration conversion.

8. (Previously Presented) The solid state energy converter of claim 17, wherein the emitter region comprises a metal or a highly doped semiconductor.

9-11. (Cancelled)

12. (Previously Presented) The solid state energy converter of claim 17, wherein the p^* doping concentration of the p-type barrier layer relates to the n doping concentration of the gap region *as* $p_i > n_i\,(m^*_p/m^*_n)$, where m^*_p is the effective mass of holes, m^*_n is the effective mass of electrons, and subscript i denotes ionized fraction of carriers at a given temperature.

13. (Original) The solid state energy converter of claim 2, wherein the collector region comprises an additional injection barrier layer with a carrier concentration p^{**} that is adjacent to the gap region to reduce a thermoelectric back flow component.

14. (Previously Presented) The solid state energy converter of claim 2, wherein the collector region comprises an additional compensation layer with acceptor concentration p^* serving as a blocking layer at a cold side of the converter, and the acceptor concentration p^* being the same as the donor concentration in the gap region.

15. (Previously Presented) The solid state energy converter of claim 2,

wherein the collector region comprises two *p*-type layers, one layer with a carrier concentration p^* serving as a blocking layer at a cold side of the converter, and the other layer with a carrier concentration p^{**} serving as an additional injection barrier layer and being adjacent to the gap region to reduce a thermoelectric back flow component.

16. (Original) The solid state energy converter of claim 13, wherein the p^{**} doping concentration of the additional injection barrier layer relates to the *n* doping concentration of the gap region as $p_i > n_i (m^*_p / m^*_n)$, where m^*_p is the effective mass of holes, m^*_n is the effective mass of electrons, and subscript *i* denotes ionized fraction of carriers at a given temperature.

17. (Currently Amended) A solid state energy converter with *n*-type conductivity, comprising:

an emitter region in thermal communication with a hot heat exchange surface, the emitter region comprising an *n*-type region with donor concentration n^* for electron emission; a *p*-type barrier layer with acceptor concentration p^* in contact with the emitter region; and

and a segmented gap region in contact with the *p*-type barrier layer and comprising a first layer of an *n*-type semiconductor material, and a second layer of a ~~metal or~~ a different highly *n*-doped semiconductor material, the second layer reducing heat flow density, wherein the *p*-type barrier laver provides a potential barrier and a Fermi level discontinuity between the emitter region and the segmented nap region.

18. (Original) The solid state energy converter of claim 17, further comprising a first ohmic contact in electrical communication with the emitter region.

19. (Original) The solid state energy converter of claim 17, further comprising a second ohmic contact in electrical communication with the gap region.

20. (Original) The solid state energy converter of claim 17, wherein the first layer is at least 1 electron scattering length wide.

21. (Original) The solid state energy converter of claim 17, wherein the first layer is at least 5 electron scattering lengths wide.

22. (Currently Amended) A solid state energy converter with *p*-type conductivity, comprising:

an emitter region in thermal communication with a hot heat exchange surface, the emitter region comprising a *p*-type region with acceptor concentration p^* for hole emission;

a semiconductor gap region with an acceptor doping *p*, the gap region in electrical and thermal communication with the emitter region, wherein the gap region is segmented and comprises a first layer of a[[n]] *p*-type semiconductor material and a second layer of ~~a metal or~~ a different highly doped *p*-type semiconductor material; and

an *n*-type barrier layer with donor concentration n^* in contact with the emitter region and with the gap region, the *n*-type barrier layer providing a potential barrier and Fermi-level discontinuity between the emitter region and the gap region.

23. (Previously Presented) The solid state energy converter of claim 22, further comprising a collector region in thermal communication with a cold heat exchange surface, the collector region being in electrical and thermal communication

with the gap region.

24. (Previously Presented) The solid state energy converter of claim 23, wherein the gap region is adjacent to the collector region.

25. (Original) The solid state energy converter of claim 23, further comprising a first ohmic contact in electrical communication with the emitter region.

26. (Original) The solid state energy converter of claim 25, further comprising a second ohmic contact in electrical communication with the collector region.

27. (Original) The solid state energy converter of claim 26, wherein the first and second ohmic contacts close an electrical circuit through an external load for heat to electricity conversion.

28. (Original) The solid state energy converter of claim 26, wherein the first and second ohmic contacts close an electrical circuit through an external power source for electricity to refrigeration conversion.

29. (Previously Presented) The solid state energy converter of claim 22, wherein the gap region is at least 1 carrier scattering length wide.

30. (Original) The solid state energy converter of claim 22, wherein the gap region is at least 5 carrier scattering lengths wide.

31. (Currently Amended) A solid state energy converter, comprising:
a thermal diode stack comprising:

a first diode with a design structure of $n^*/p/n$ on a hot side of the converter, the n^* representing a *n*-type emitter region with a donor concentration n^*, the *p* representing a *p*-type barrier region with an acceptor concentration *p*, and the *n* representing a *n*-type

segmented gap region with a donor concentration *n* and comprising a first layer of an *n*-type semiconductor material and a second layer of ~~a metal or~~ a different highly doped *n*-type semiconductor material, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region;

a plurality of diodes having the same structure as the first diode and connected with the first diode; and

an n^* layer that terminates the plurality of diodes on a cold side of the converter ~~with~~.

32. (Currently Amended) A solid state energy converter, comprising:

a thermal diode stack comprising:

a first diode with a design structure of $n^*/p/n/p_c$, on a hot side of the converter, the n^* representing an *n*-type emitter region with a donor concentration n^*, the *p* representing a *p*-type barrier region with an acceptor concentration *p*, the *n* representing a segmented *n*-type gap region with a donor concentration *n* and comprising a first layer of an *n*-type semiconductor material and a second layer of ~~a metal or~~ a different highly doped *n*-type semiconductor material, and the p_c representing a *p*-type compensation layer acting as a collector blocking barrier with acceptor concentration p^*, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with an n^* layer.

33. (Currently Amended) A solid state energy converter, comprising: a thermal diode stack comprising:

a first diode with a design structure of $n^*/p/n/p_i$ on a hot side of the converter, the n^* representing an n-type emitter region with a donor concentration n^*, the p representing a p-type barrier region with an acceptor concentration p, the n representing a segmented n-type gap region with a donor concentration n and comprising a first layer of an n-type semiconductor material and a second layer of ~~a metal or~~ a different highly doped n-type semiconductor material, and the p_i representing an additional p-type barrier region with an acceptor concentration p^{**}, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with an n^* layer.

34. (Previously Presented) A solid state energy converter, comprising:

a thermal diode stack comprising: a first diode with a design structure of $n^*/p/n/p_i/p_c$ on a hot side of the converter, the n^* representing a n-type emitter region with a donor concentration n^*, the p representing a p-type barrier region with an acceptor concentration p, the n representing a n-type gap region with a donor concentration n, the p_i representing an additional p-type barrier region with a donor concentration p^{**}, and the p_c, representing a p-type compensation layer acting as a collector blocking barrier with a donor concentration of p^*, wherein the barrier layer is

configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with an n^* layer.

35. (Currently Amended) A method for converting thermal energy to electric energy, or electric energy to refrigeration, comprising:

injecting carriers into an *n*-type gap region from a highly doped n^* emitter region through a *p*-type barrier layer positioned between the emitter region and the gap region, wherein:

the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

the gap region is segmented and comprises a first layer of an *n*-type semiconductor material and a second layer of ~~a metal or~~ a different highly doped *n*-type semiconductor material;

allowing for discontinuity of corresponding Fermi-levels; and

forming a potential barrier to sort electrons by energy.

36. (Currently Amended) A method for converting thermal energy to electric energy, or electric energy to refrigeration, comprising:

injecting carriers into a *p*-type gap region from a highly doped p^* emitter region through an *n*-type barrier layer positioned between the emitter region and the gap region, wherein:

the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

the gap region is segmented and comprises a first layer of an n-type semiconductor material and a second layer of ~~a metal or~~ a different highly doped *n*-type semiconductor material;

allowing for discontinuity of corresponding Fermi-levels; and

forming a potential barrier to sort electrons by energy.

37. (Previously Presented) A solid state energy converter, comprising:

a thermal diode stack comprising: a first diode with a design structure of $p^*/n/p/n_i/n_c$ on a hot side of the converter, the p^* representing *p*-type emitter region with an acceptor concentration p^*, the *n* representing an *n*-type barrier region with a donor concentration *n*, the *p* representing a *p*-type gap region with an acceptor concentration *p*, the n_i representing an additional *n*-type barrier region with a donor concentration n^{**}, and the n_c, representing an *n*-type compensation layer acting as a collector blocking barrier with a donor concentration of n^*, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with a p^* layer.

2. The following is an examiner's statement of reasons for allowance: The thermoelectric element of JP 2001-217469 (JP '469), has a structure with repeating p-type and n-type semiconductor materials, which does not anticipate or render obvious

the structure in independent claims 17, 22, 31, 32, 33, 35, and 36, which includes a segmented gap region including a first layer of n-type (or p-type) semiconductor material and a second layer of a different highly n-doped (or p-doped) semiconductor material, and wherein the recited p-type (or n-type) barrier layer provides a potential barrier and a Fermi level discontinuity between the recited emitter region and the segmented gap region. Simply put, JP '469's pnpn(etc) structure cannot and does not anticipate or render obvious the instantly claimed structure which includes a segmented gap of, for example, nn or pp wherein the second layer of the gap is a different highly n-doped (for said nn gap) or p-doped (for said pp gap) semiconductor material. JP '469's pnpn(etc) structure clearly does not teach or suggest the design structure in instant claims 34 and 37.

Kucherov et al, "Study of Emitter Structures for InSb Thermal Diodes," 22nd International Conference of Thermoelectrics, (2003), pages 578-581 (which is already of record), teaches an n^*pnc diode wherein (c) is taught as being n-p-n^* (see page 578). Thus, the actual structure would be n^*pnpn*. One skilled in the art would expect the respective n and n^* layers to be made of the same material with different doping concentration, and thus, there would not be a segmented gap comprising a first n-type layer followed by a second layer of a different highly n-doped semiconductor material. Furthermore, while Kucherov et al does discuss Fermi level (see Figure 2), there is no specific teaching Fermi level discontinuity as in instant claims 17, 22, 31, 32, 33, 35, and 36. The importance of the Fermi level discontinuity is that it permits sorting electrons by energy (see paragraph 0016). The advantage of the segmented gap

having a different highly doped semiconductor material is that this reduces heat flow density (see paragraph 0040). Even if Kucherov et al's device structure was n^*pnn^*pn (i.e., the collector (c) is n^*pn rather than npn^*), the instant device would still not be obtained because, once again, one skilled in the art would expect the respective n and n^* layers to be made of the same material with different doping concentration, and thus, there would not be a segmented gap comprising a first n-type layer followed by a second layer of a different highly n-doped semiconductor material. Likewise, the advantage of the segmented gap having a different highly doped semiconductor material is that this reduces heat flow density (see paragraph 0040). Such is not taught or suggested by Kucherov et al.

Kucherov et al clearly does not teach or suggest the design structure in instant claims 34 and 37.

The following reference is hereby made of record: Kucherov et al, "Importance of Barrier Layers in Thermal Diodes for Energy Conversion," Journal of Applied Physics, Vol. 97, (2005), pages 1-8.

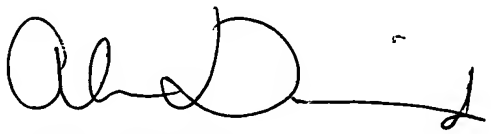
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan Diamond whose telephone number is 571-272-

1338. The examiner can normally be reached on Monday through Friday, 5:30 a.m. to 2:00 p.m. ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alan Diamond
Primary Examiner
Art Unit 1753

Alan Diamond
April 24, 2006